

Fabrication Techniques for Thermoelectric Devices Based on Nanostructured Silicon

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We discuss processes for the fabrication of devices for thermoelectric generation, based on silicon nanostructures. The main issue that we address is the design and development of fabrication processes for devices exploiting a large number of interconnected nanostructures. Such devices are characterized by good mechanical strength and at the same time they can handle large currents and deliver high power. First, techniques based on lithography and conventional CMOS processing are presented. These techniques allow the fabrication of suspended silicon masses, connected with the silicon substrate through nanomembranes. Then, a low-cost process for the fabrication of forests of long silicon nanowires is presented. Finally, a technique for the fabrication of a contact at the top of this silicon nanowire forest is reported and discussed.

Keywords: Silicon Nanowires, Thermoelectric Generator.

1. INTRODUCTION

In the last few years, several experimental^{1–3} and theoretical studies^{4,5} have demonstrated that the thermal conductivity k_t is strongly reduced in silicon nanostructures, while their electrical conductivity σ and Seebeck coefficient S remain comparable with those of bulk silicon. A suppressed thermal conductivity enhances the main thermoelectric figure of merit $Z = S^2\sigma/k_t$, which can reach values of interest for the efficient direct conversion of heat into electrical power. Hence, nanostructuring offers interesting opportunities for the fabrication of thermoelectric devices based on a material (silicon), which is abundant in the Earth's crust, biocompatible and at the basis of the electronic industry. Devices based on silicon nanowires have been fabricated by many research groups using different techniques,^{6–8} and many efforts have been dedicated to the study of the thermal conductivity of such nanostructures.^{9–11}

It has been demonstrated that the key factor for the reduction of k_t is phonon surface scattering: rough nanowires,^{12–15} with a diameter between 50 and 100 nm, have shown a strongly reduced value of kt , below 10 W/mK. Conversely, the electrical conductivity of nanowires wider than 50 nm is only slightly affected by surface scattering, in particular in heavily doped

nanostructures.¹⁶ If the thermal conductivity is reduced down to the order of 1 W/mK, thermoelectric performances can be enhanced by optimizing the nanowire doping.¹⁷ So far, the potential for thermoelectric applications of nanostructured silicon have been demonstrated with devices based on one, or very few, nanowires. The practical exploitation of these properties requires the development both of architectures and of reliable processes for the large-scale fabrication of devices made up of a large collection of nanostructures, placed in suitable configurations. We present technological solutions for the fabrication of silicon devices whose active part consists of millions of nanostructures. These devices are completed with electrical and thermal contacts, so that several similar structures (with complementary doping) can be interconnected to make a complete thermoelectric generator. Two main problems need to be addressed. First, a thermoelectric generator must be able to supply significant power, therefore nanostructures must be as wide as possible, to the extent allowed by the need to keep thermal conductivity low. Moreover, the length of the nanostructures must be as large as possible to achieve a good thermal separation between the hot and cold heat sources. This implies that the issue of mechanical stability has to be taken into consideration, because nanowires need to be free from any contact to the substrate or holder, whose parallel heat conduction would degrade the thermoelectric performance.

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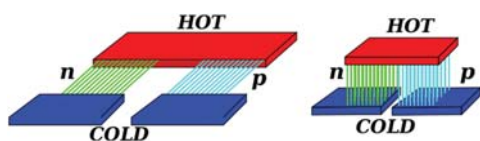


Figure 1. Sketches of horizontal (suspended) Si nanostructures, which can be fabricated by means of advanced lithography (on the left), and vertical Si nanostructures, which can be obtained by means of highly anisotropic silicon etching (on the right).

We report on two different approaches, represented in the sketches of Figure 1: the planar strategy and the vertical strategy.

The planar structure shown on the left can be fabricated by means of advanced lithography and etching, exploiting standard Si processes that are currently used for Integrated Circuit (IC) fabrication; therefore, this strategy can be proposed for large scale integration. The nanostructures need to be suspended between the cold and hot sections of the generator. In Section 2, approaches for the fabrication of devices based on suspended nanostructures (silicon nanomembranes) will be presented. A first application of these devices can be as test structures for the measurement of thermal conductivity. Moreover, as they require standard IC fabrication techniques, these thermoelectric modules could be integrated together with the circuits to which they will supply power. In Section 3 we will instead discuss a maskless process for the top-down fabrication of silicon nanowire forests, perpendicular to the silicon substrate and with a height of several tens of micrometers (see the sketch on the right of Fig. 1). These nanowire forests can be obtained by means of a highly directional vertical etching applied to a silicon wafer. We used the Metal Assisted Etching technique, which is very simple and low-cost, and enables the fabrication of dense forests of nanowires, narrower than 100 nm. Other techniques, such as the vertical growth by means of Low Pressure Chemical Vapor Deposition (LPCVD), could be considered.

The crucial point of the vertical strategy is to fabricate a common contact to the top ends of the nanowires, since the bottom contact is provided by the silicon substrate itself. The main focus of Section 3 is the presentation of a technique, based on electrodeposition, which enables the selective growth of copper on the top of a silicon nanowire forest.

2. SI NANOMEMBRANES DEFINED BY MEANS OF LITHOGRAPHY

Advanced lithography can be used for the top-down fabrication of silicon nanostructures.

It has been demonstrated¹⁸ that regular arrays of silicon nanowires, fabricated by means of *e*-beam lithography and etching on a Silicon On Insulator (SOI) substrate, are equivalent, from the point of view of the electrical and thermal resistances, to millimeter long silicon nanowires,

and the presence of multiple interconnections can make them very reliable with respect to the failure of several nanowires. This solution is compatible with standard CMOS processing. In particular, optical lithography, currently available for modern integrated circuit fabrication, is capable of defining features with widths well below 50 nm. Therefore, nanostructures with a width in the 50–100 nm range, that have a reduced thermal conductivity and an electrical conductivity comparable to that of bulk silicon, can be easily fabricated. However, lithography is a planar process, which allows the definition of a single layer of silicon nanowires, arranged on a substrate. Since nanowires have a low mechanical stiffness, the substrate cannot be removed, and thus the efficiency is reduced by its contribution to the thermal conduction. Moreover, although a cross section of the device can contain thousands of nanowires 50–100 nm wide, the current (and, as a consequence, the power) that the device can deliver is still too low, even for applications such as energy scavenging, in which a few milliwatts can be sufficient. The parallel heat conduction of the substrate can be avoided by using suspended structures. Silicon masses suspended by means of CVD-grown nanowires^{19,20} have been fabricated in the past. An improved mechanical stability and a larger cross-section for current conduction can be obtained by using nanomembranes instead of nanowires, even though the reduction of the thermal conductivity can be less effective than in nanowires. Figure 2 illustrates the fabrication process for a silicon device consisting of a suspended central mass, laterally held by thin silicon nanomembranes, which are parallel to the substrate. The process is based on a Silicon On Insulator (SOI) wafer and it is similar to that used for the fabrication of silicon nanowire networks, previously reported.¹⁸ The thickness of the top silicon layer, which can eventually be reduced by means of etching, determines the final thickness of the nanomembranes: phonon surface scattering is more effective in thinner nanomembranes. A mask, consisting of a thin SiO₂ layer (grown on the top) or of a metal film, is fabricated on the top of the silicon layer by means of advanced lithography (see step I in the sketch of Fig. 2). To be noted that the reduction of the thermal conductivity relies on the reduced thickness of the nanomembranes. Therefore, relaxed lithography can be used for the definition of the nanomembrane width (although in this work *e*-beam lithography has been used for rapid prototyping). The mask is used for the selective anisotropic etching of silicon (see step II), which defines the silicon nanostructures. The windows opened in the top silicon layers allow the etching of the buried SiO₂ (see step III). In this case, an isotropic etching (buffered HF) is used, so that the silicon dioxide is removed also underneath the nanostructures, in such a way as to make them suspended, as shown in Figure 2 (see step III). Figure 3 reports SEM images of a typical device, fabricated following the process shown in Figure 2. The SEM photo on the right of Figure 3 is

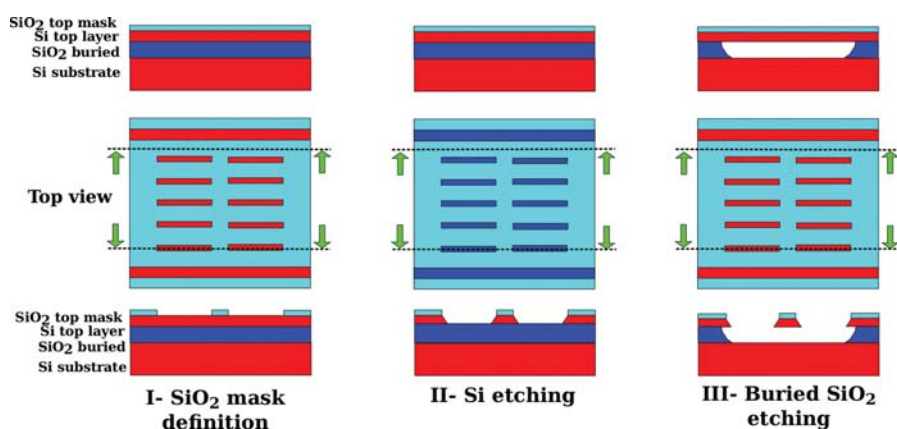


Figure 2. Sketch of the three main process steps for the fabrication of horizontal silicon nanomembranes.

a top view of the silicon nanomembranes, which are parallel to the substrate, arranged in a comb configuration. The darker regions are windows in the top silicon layer, which have been used to etch the buried oxide. A possible application of this device can be the measurement of the thermal conductivity of the nanomembranes, by means of the 3ω technique.²¹ For this purpose, a heater is fabricated on the central suspended mass before the isotropic oxide etching used for the suspension of the nanomembranes. The heater consists of a metal strip, exactly aligned in the middle of the comb (see the SEM photo on the right of Fig. 3). The fabrication of the heater has been performed by means of a lithographic step properly aligned with the silicon nanostructures. Electron beam lithography with Poly Methyl Methacrylate resist has been used in this step. After resist development, a metal film has been deposited by means of thermal evaporation. The metal film consists of a layer of chromium 10 nm thick, for adhesion on silicon, a layer of gold 80 nm thick and another final thin layer of chromium (15 nm thick) for protection. After thermal evaporation, metal lift-off has been performed in

hot acetone. In the picture on the left of Figure 3, the four-probe configuration of the tracks used for contacting the suspended heater can be seen. The 3ω measurement is made injecting a sinusoidal current between two probes, and measuring the voltage drop between the other two probes, by means of a lock-in amplifier. The amplitude of the third harmonic is related to the thermal conductivity of the nanomembranes. However, an accurate model for thermal transport in the suspended membranes needs to be developed for extracting the correct value of the thermal conductivity from the experimental measurements. It must be noted that the development of proper modelling is the most difficult task of the 3ω technique. We have applied a simple one-dimensional model, obtaining a thermal conductivity of 86.4 W/mK for nanomembranes 240 nm thick and of 54.5 W/mK for nanomembranes 140 nm thick. These values are consistent with the theoretical Casimir limit,²² valid for smooth nanomembranes, and are close to those reported by other authors.²³ However, our simple one-dimensional model is not very accurate and significant errors are possible; a more accurate model is still

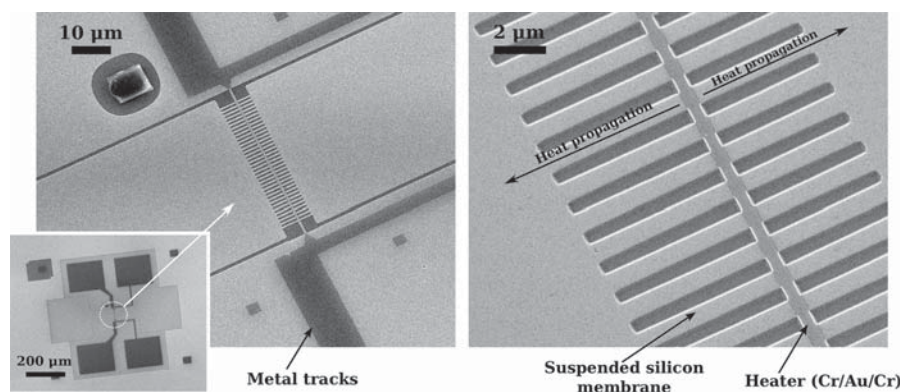


Figure 3. SEM images of planar silicon nanomembranes, fabricated on a SOI substrate following the sketches of Figure 2. A heater, made of metal film (Cr/Au/Cr), has been fabricated on the central suspended mass. The device is completed with the deposition of metal tracks and pads needed for external connections.

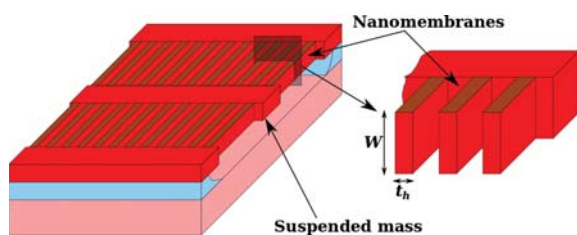


Figure 4. Sketch of a device based on silicon nanomembranes perpendicular to the substrate. The enlargement on the right shows a cross-section of a few nanomembranes, whose thickness t_h is defined in the lithographic step, while the width W is determined by the depth achievable with plasma etching.

under development. These values of thermal conductivity are comparable to those measured with smooth nanowires 240 nm and 140 nm wide. For nanowires, it has been demonstrated that a strong reduction of the thermal conductivity is achievable increasing the surface roughness.

A denser packing of the silicon nanomembranes, yielding a larger total cross-section for current conduction within the same die area, and an improved mechanical stability, can be obtained if the nanomembranes are arranged in a perpendicular direction with respect to the silicon substrate, as shown in the sketch of Figure 4. To this end, a highly selective dry plasma etching (Reactive Ion Etching, RIE) must be used in the process step II of Figure 2. Since the plasma silicon etching technique that we used is not selective with respect to silicon dioxide, a metal etch mask

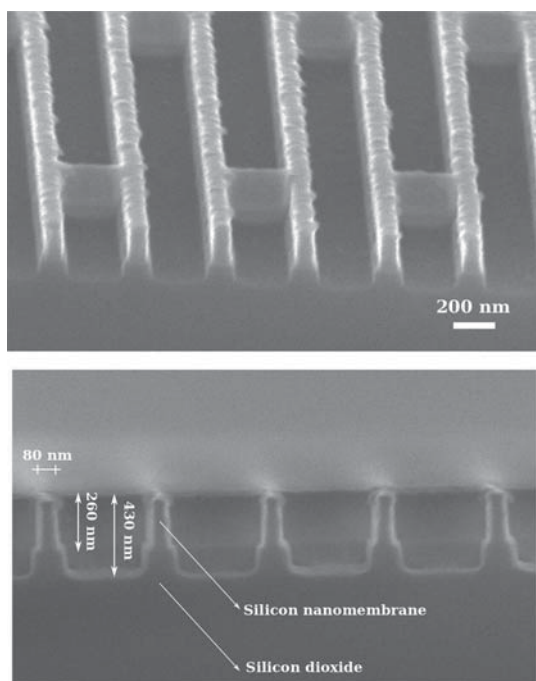


Figure 5. Cross sections of vertical silicon nanomembranes, before the BHF under-etch.

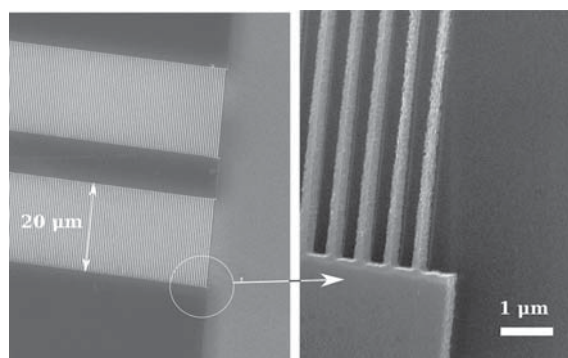


Figure 6. SEM photos of a prototype of a thermoelectric generator, based on a suspended central mass, held by silicon nanomembranes. On the left: view of the overall device. On the right: a detail of the suspended membranes.

must be defined in the lithographic step (step I), whose resolution determines the minimum achievable nanomembrane thickness. The nanomembrane width is determined by the maximum depth (maximum aspect ratio) achievable with the plasma etching procedure (see Fig. 2). The thickness of the top silicon layer should be chosen according to the dry etch capabilities. Cross-sections of silicon nanomembranes are shown in the SEM images of Figure 5. The thickness of the top silicon layer is 260 nm. The plasma etching has been performed in Freon (CF_4) with an RF power of 300 W for 3', and with a residual pressure of 2.6×10^2 Pa (parameters are machine dependent). Before the etching process, an aluminum mask 80 nm thick has been defined by means of *e*-beam lithography, metal thermal evaporation and lift off in hot acetone. It can be seen that the etch time is more than enough for reaching the silicon dioxide buried layer, for a total etch depth of 430 nm. Therefore, the aspect ratio is about 5:1. Standard dry etching cannot reach an aspect ratio greater than 10:1, while it has been demonstrated that aspect ratios larger than 100:1 can be achieved by means of advanced Deep-RIE,^{24–26} even with structures as narrow as 100 nm. The suspension of the nanomembrane is obtained by etching the buried oxide away. Figure 6 includes SEM photos of a prototype, fabricated following the sketch of Figure 4. The left panel provides a view of the overall device, while the right panel contains a detail with a few suspended nanomembranes attached to the silicon body.

3. VERTICAL SILICON NANOWIRE FORESTS

Highly directional RIE can be used for the fabrication of silicon nanowires which are perpendicular to the silicon substrate (see the sketch on the right of Fig. 1). However, the maximum length of the nanowires achievable with the largest aspect ratio (100:1, which corresponds to a nanowire length of 10 μm for a width of 100 nm) would not be sufficient for the thermal separation of the hot and

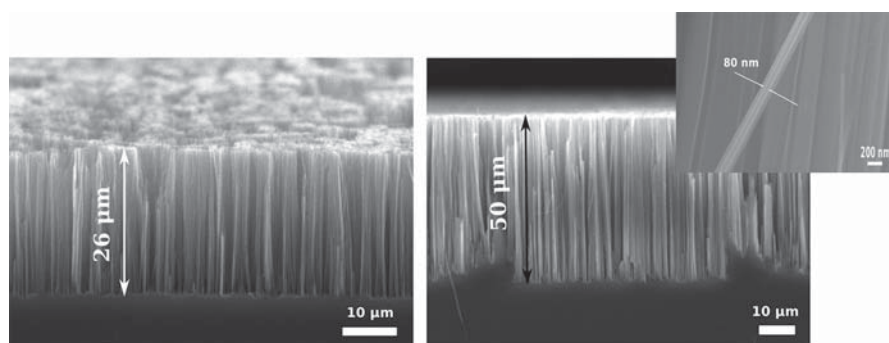


Figure 7. Left panel: SEM image of the cross-section of a silicon nanowire forest, obtained with a 120' etch in HF:AgNO₃:H₂O 16:5:60 in volume. Right panel: SEM image of a cross-section of a silicon nanowire forest, obtained with a 240' etch in HF:AgNO₃:H₂O 16:2:60 in volume.

cold part of the generator. Higher aspect ratios can be achieved by means of bottom-up approaches, such as epitaxial growth, which can be performed, for example, with low pressure chemical vapor deposition.^{27–29} Alternatively, maskless top-down etch can be performed by means of Metal assisted Chemical Etching (MaCE).^{30,31} This well known wet etching technique is based on the local oxidation of silicon, catalyzed by metal particles, in a solution that contains an oxidizing agent (as H₂O₂), together with hydrofluoric acid (HF) that removes the generated silicon dioxide.

The metal particles, deposited on the top of a silicon substrate, sink into the silicon as the etch proceeds, therefore silicon crystalline nanowires are left in the regions among the particles. Metal nanoparticles can be fabricated by means of thermal evaporation of a thin layer of Au or Ag on a silicon wafer, and a successive annealing process. Alternatively, metal ions can be provided using a salt, such as for example silver nitrate (AgNO₃), as oxidizing agent. In this case the process is very simple, because it is sufficient to soak a silicon wafer in a diluted solution of HF:AgNO₃:H₂O. The concentration of reagents and the etch time determine the average diameter and the length of

the nanowires. As an example, Figure 7 shows the comparison between two silicon nanowire forests fabricated with different etch times and reagent concentrations. Longer nanowires can be achieved using a lower silver nitrate concentration and a longer etch time. As shown in the left panel of Figure 7, a length in excess of 50 μm, with an average nanowire width of 100 nm, can be obtained.

The nanowire density is very high, of the order of 10⁷ nanowires/mm², which is a key point in applications for thermoelectric purposes. This technique is very simple and low-cost, therefore suitable for industrial, large scale, applications. However, further research efforts are needed to obtain samples with good uniformity and repeatability over large areas.³²

The key point for the fabrication of a thermoelectric generator is to provide reliable top and bottom contacts to the nanowire forest. The bottom contact is straightforward because the nanowires are anchored to the silicon substrate which is a good thermal and electrical conductor. The difficult task is to connect all the top ends of the nanowires, with the fabrication of a common top contact. A further complication is given by the non uniformity of the nanowire length, which has a dispersion of few

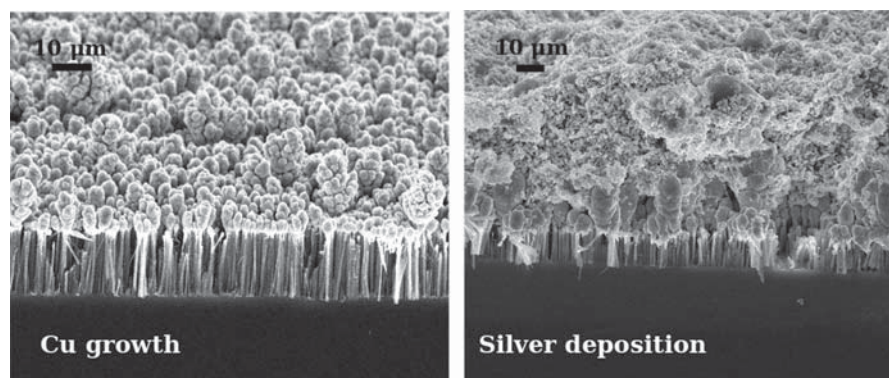


Figure 8. Left panel: SEM image of a cross-section of a silicon nanowire forest, after a selective growth of copper on the top of the nanowires by means of electrodeposition (see the text for the electrodeposition details). Right panel: after Cu electrodeposition, an almost uniform contact is obtained by depositing silver with a colloidal solution.

micrometers. Moreover, the top ends of the nanowires tend to group in bundles. We have developed a technique that appears promising, which consists in the selective growth of copper on top of the nanowires, by means of Cu electrodeposition. At first, metal thermal evaporation is used for the deposition of a Cr thin layer 15 nm thick, which provides good adhesion to silicon, and a Cu layer 20 nm thick, to be used as a seed for the electrodeposition. As thermal evaporation is a directional process, the metal film is mainly deposited on top of the nanowires. Electrodeposition is performed in a $\text{H}_2\text{SO}_4\text{:CuSO}_4$ aqueous solution (19.62 g of H_2SO_4 , 12.77 g of CuSO_4 in 200 ml deionized water),³³ using the nanowire forest as the negative electrode. The positive counter electrode is made of copper. The electrolytic cell is designed in such a way that only the top of the nanowires is in contact with the solution, while the bottom of the silicon substrate is contacted outside the solution. Figure 8 shows a typical outcome of copper electrodeposition, performed for 5' with a current density of 500 A/m².

The selective growth of copper on the top of the nanowires can be seen in the SEM image on the left. Although the copper layer appears chaotic, its electrical resistivity, measured with the four-probe technique, turned out to be comparable with that of a continuous Cu film, which is of the order of a few $\mu\Omega\text{m}$. A more uniform surface, for a better electrical and thermal contact, can be obtained with a further deposition of metal, such as, for example, silver, as shown in the right SEM image of Figure 8.

4. CONCLUSIONS

We have presented technological processes for the fabrication of silicon devices based on a large number of interconnected nanostructures. Since the thermal conductivity of nanostructured silicon can be significantly suppressed with respect to the bulk value, these devices are potential candidates for a direct thermal-to-electrical energy conversion, with efficiencies comparable to those achievable with other materials, such as tellurium compounds. Therefore nanostructuring has a potential to enable, for thermoelectric applications, the usage of silicon, which is the second most abundant element in Earth's crust (conversely, tellurium is almost as rare as platinum), is very well known from the technological point of view and is biocompatible (tellurium is very poisonous and a source of pollution).

In particular, we have reported a planar process fully compatible with CMOS technology. Thin silicon nanomembranes, arranged perpendicularly to the silicon substrate, have been fabricated by means of reactive ion etching. A large number of parallel nanomembranes can be obtained with this process and buried oxide underetching makes their suspension possible, so that a parallel heat conduction in the substrate can be avoided. These nanostructures could possibly be exploited for energy scavenging from low temperature heat sources. Electronic

circuits can be integrated together with thermoelectric generators powering them. The second technological process that we present is based on metal-assisted chemical etching that allows the fabrication of forests of silicon nanowires with a high aspect ratio. A technique for the fabrication of the top contact, to be used both for thermal and for electrical conduction, has been illustrated. This process is simple and cheap, and is suitable for large scale production of silicon-based thermoelectric generators. However, a considerable experimental effort is still needed in order to obtain a good uniformity of silicon nanowire forests over a large area.

Further experimental work is also needed in terms of the accurate measurement of the thermoelectric figure of merit and, in particular, of the suppression of the thermal conductivity actually achieved in optimized silicon nanomembranes and nanowires. Knowledge of these quantities is needed to perform a detailed assessment of the application potential of the proposed structures.

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